

#### INVENTOR INFORMATION

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#### APPLICATION INFORMATION

Title Line One:: Layout Technique for Matched Resistors o  
Title Line Two:: n an Integrated Circuit Substrate  
Total Drawing Sheets:: 9  
Formal Drawings?: No  
Application Type:: Utility  
Docket Number:: 1875.2330005  
Secrecy Order in Parent Appl.?: No

#### CONTINUITY INFORMATION

This application is a:: CONTINUATION OF  
> Application One:: 10/208,043  
Filing Date:: 07-31-2002

Which is a::NON PROV. OF PROVISIONAL  
>> Application Two:: 60/350,035  
Filing Date:: 01-23-2002

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